UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

TELEPUTERS, LLC, Plaintiff v. RENESAS ELECTRONICS AMERICA, INC. AND RENESAS ELECTRONICS CORPORATION, Defendants	**Case No. 6:20-cv-599** **JURY TRIAL DEMANDED**

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Teleputers, LLC ("Plaintiff" or "Teleputers") hereby files this Original Complaint for Patent Infringement against Defendants Renesas Electronics America, Inc. and Renesas Electronics Corporation (collectively "Defendants" or "Defendant" or "Renesas"), and alleges, on information and belief, as follows:

THE PARTIES

1. Teleputers, LLC is a limited liability company organized and existing under the laws of the State of New Jersey with its principal place of business in Princeton, New Jersey.

2. On information and belief, Defendant Renesas Electronics America, Inc. is a California corporation with its principal place of business at 1001 Murphy Ranch Road, Milpitas, California 95035. Renesas Electronics America, Inc. may be served through its registered agent, Corporation Service Company (which will do business in California as CSC - Lawyers Incorporating Service, 251 Little Falls Drive, Wilmington, Delaware 19808.

3. On information and belief, Defendant Renesas Electronics Corporation is a company organized under the laws of Japan with its principal place of business at TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan. Renesas Electronics Corporation may be served through its U.S. subsidiary, Renesas Electronics America, Inc.

JURISDICTION AND VENUE

4. This action arises under the patent laws of the United States, 35 U.S.C. § 1, *et seq*. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

5. Defendants have committed acts of infringement in this judicial district.

6. On information and belief, Defendants maintain regular and systematic business interests in this district and throughout the State of Texas including through their representatives, employees and physical facilities.

7. On information and belief, the Court has personal jurisdiction over Defendants because Defendants have committed, and continue to commit, acts of infringement in the State of Texas, have conducted business in the State of Texas, and/or have engaged in continuous and systematic activities in the State of Texas. On information and belief, Defendants' accused instrumentalities that are alleged herein to infringe were and continue to be used, imported, offered for sale, and/or sold in the Western District of Texas.

8. On information and belief, Defendants voluntarily conduct business and solicit customers in the State of Texas and within this District, including, but not limited to, its offices located at 900 S. Capital of Texas Highway, Las Cimas IV, Suite 250, Austin, Texas 78746. *See, e.g.:*

Global Locations | Renesas Electronics Europe

Design Centers 1

Company	Phone	Fax	Email	Notes
TX Design Center 900 S. Capital of Texas Hwy Las Cimas IV, Suite 250 Austin, TX 78746	--	--	--	

Renesas website as visited on June 23, 2020 at: https://www.renesas.com/us/en/support/contact/locations.html?region=United States&subregion=Texas.

9. On information and belief, Defendants generate substantial revenue within this District and from the acts of infringement as carried out in this District. As such, the exercise of jurisdiction over Defendants would not offend the traditional notions of fair play and substantial justice.

10. Venue is proper in the Western District of Texas pursuant to 28 U.S.C. § 1400(b) and 28 U.S.C. § 1391(c)(3).

NOTICE OF TELEPUTERS' PATENTS

11. Teleputers is owner by assignment of U.S. Patent No. 6,922,472 ("the '472 Patent") entitled "Method and system for performing permutations using permutation instructions based on butterfly networks." A copy may be obtained at: https://patents.google.com/patent/US6922472B2/en.

12. Teleputers is owner by assignment of U.S. Patent No. 6,952,478B2 ("the '478 Patent") entitled "Method and system for performing permutations using permutation instructions based on modified omega and flip stages." A copy may be obtained at:

https://patents.google.com/patent/US6952478B2/en.

13. Teleputers is owner by assignment of U.S. Patent No. 7,092,526B2 ("the '526 Patent" and collectively with the '478 Patent, "the Patents-in-Suit") entitled "Method and system for performing subword permutation instructions for use in two-dimensional multimedia processing." A copy may be obtained at: https://patents.google.com/patent/US7092526B2/en.

14. Teleputers is owner by assignment of U.S. Patent No. 7,174,014B2 ("the '014 Patent") entitled "Method and system for performing permutations with bit permutation instructions." A copy may be obtained at: https://patents.google.com/patent/US7174014B2/en.

15. Teleputers is owner by assignment of U.S. Patent No. 7,519,795B2 ("the '795 Patent") entitled "Method and system for performing permutations with bit permutation instructions." A copy may be obtained at: https://patents.google.com/patent/US7519795B2/en.

16. The foregoing Patents, namely the '014 Patent, the '526 Patent, the '478 Patent, the '472 Patent, and the '795 Patent are collectively referred to as "the Teleputers Patents."

17. The Teleputers Patents are valid, enforceable, and were duly issued in full compliance with Title 35 of the United States Code.

18. Defendants, at least by the date of this Original Complaint, are on notice of the Teleputers Patents.

ACCUSED INSTRUMENTALITIES

19. On information and belief, Defendants make, use, import, sell, and/or offer for sale a multitude of products and services as systems on chips ("SoC") that employ Arm Neon technology supporting the infringing instructions including, but not limited to: the R-Car Hxx, R-Car Mxx, R-Car Exx, R-Car V3M, EMMA Mobile/EV2, R-Mobile A1, RZ/A1xx, RZ/A2M, RZ/G2xx, RZ/G1xx, GR-PEACH, GR-LYCHEE, emCON-RZ_G1x, and DIMM-RZ/A1H

(individually and collectively, the "Accused Instrumentalities"). On information and belief, the Accused Instrumentalities are made, used, sold, offered for sale, and/or imported in the United States by Defendants.

COUNT I
(Infringement of U.S. Patent No. 7,092,526B2)

20. Teleputers incorporates the above paragraphs by reference.

21. Defendants have been on notice of the '526 Patent at least as early as the date it received service of this Original Complaint.

22. On information and belief, Defendants have directly infringed and continue to infringe the '526 Patent by making, using, importing, selling, and/or, offering for sale the Accused Instrumentalities in the United States.

23. On information and belief, Defendants, with knowledge of the '526 Patent, indirectly infringe the '526 Patent by inducing others to infringe the '526 Patent. In particular, Defendants intend to induce customers to infringe the '526 Patent by encouraging customers to use the Accused Instrumentalities in a manner that results in infringement.

24. On information and belief, Defendants also induce others, including its customers, to infringe the '526 Patent by providing technical support for the use of the Accused Instrumentalities.

25. On information and belief, at all times Defendants own and control the operation of the Accused Instrumentalities in accordance with an end user license agreement.

26. On information and belief, the Accused Instrumentalities necessarily infringe one or more claims of the '526 Patent when used as intended.

27. On information and belief, the Accused Instrumentalities infringe at least Claim 1 of the '526 Patent by providing a method for permuting two-dimensional (2-D) data in a programmable

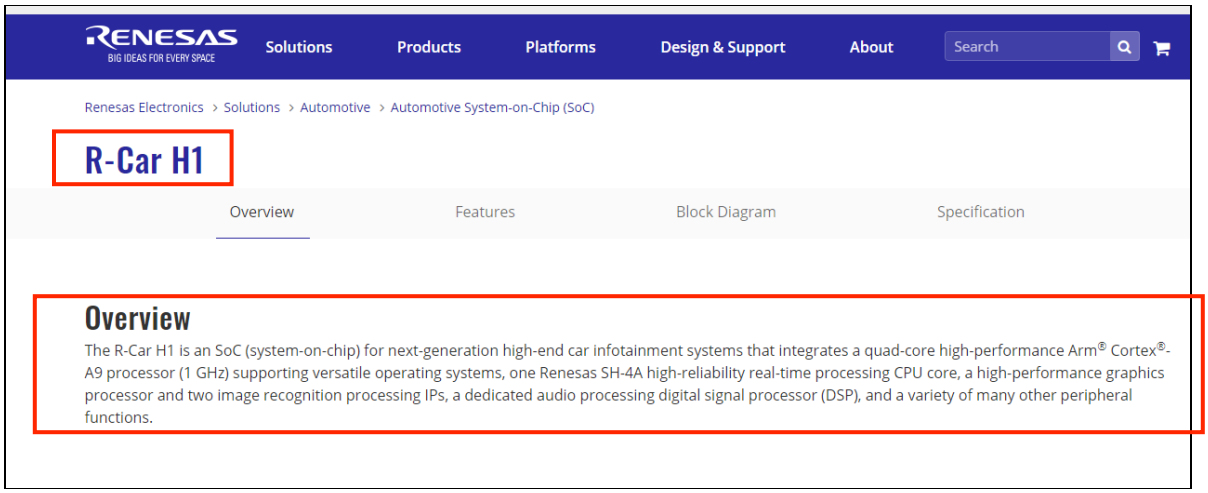
processor. For example, Defendants provide a system-on-chip (including but not limited to R-Car Hxx, R-Car Mxx, R-Car Exx, R-Car V3M, EMMA Mobile/EV2, R-Mobile A1, RZ/A1xx, RZ/A2M, RZ/G2xx, RZ/G1xx, GR-PEACH, GR-LYCHEE, emCON-RZ_G1x, and DIMM-RZ/A1H) solutions for parallel data processing.

28. For example, Defendants' R-Car H1 SoC (used herein as an exemplary product) is used for car infotainment systems. The R-Car H1 includes a quad-core Arm Cortex-A9 processor (1 GHz), a Renesas SH-4A real-time processing CPU core, a graphics processor and two image recognition processing IPs, and/or an audio processing digital signal processor (DSP).

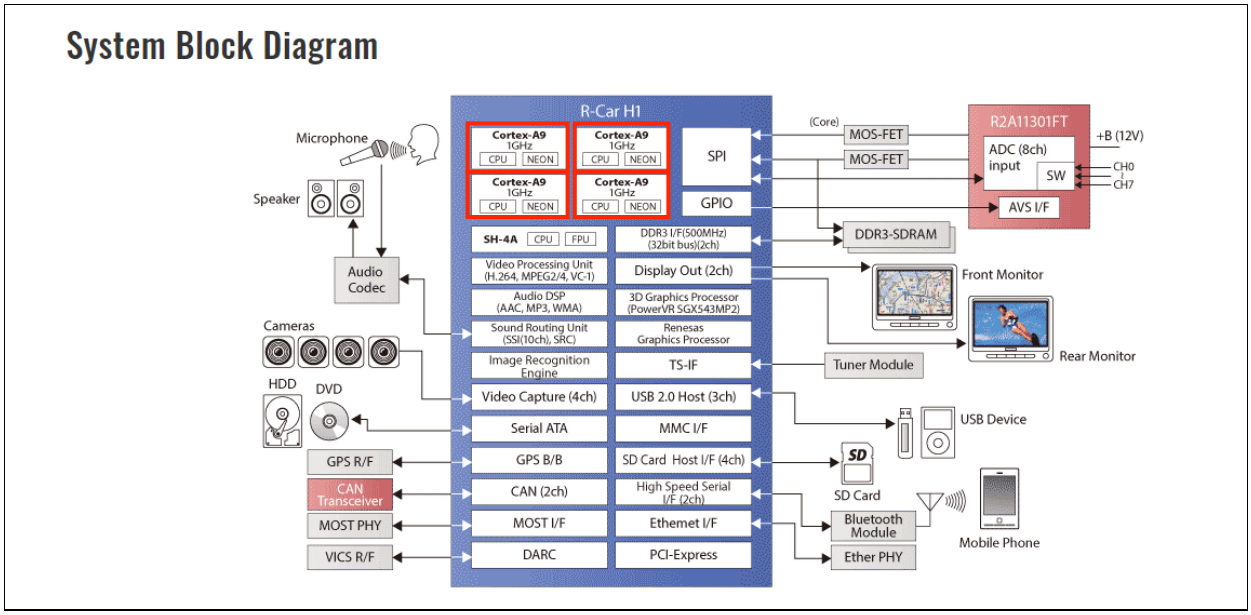
29. Further, the R-Car H1 SoC ("programmable processor") utilizes Arm Neon technology (an advanced Single Instruction Multiple Data (SIMD) architecture) for improving audio/video encoding and decoding, 2D/3D graphics ("two dimensional (2-D) data"), and/or image/video processing. ARM Neon SIMD architecture provides permutation instructions to rearrange individual elements present in 2D/3D graphics.

30. Further, on information and belief, Defendants directly infringe the claim at least when it tests its SoCs. During such tests, Defendants utilize the SoCs to perform permutation on the input data using permutation instructions available in ARM Neon SIMD ISA (Instruction Set Architecture).

31. Further, Defendants indirectly infringe the claim at least when Defendants' customers (such as device manufacturers which use Defendants' SoCs in their products) perform the method while testing their devices and when the devices are operated by end-users.



Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as visited on June 29, 2020.



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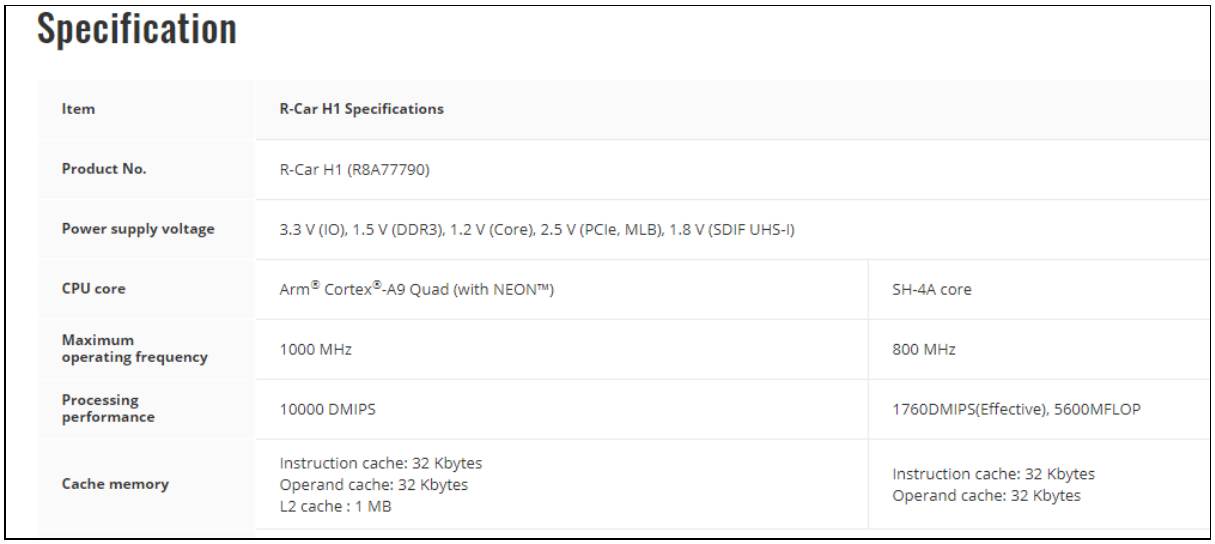
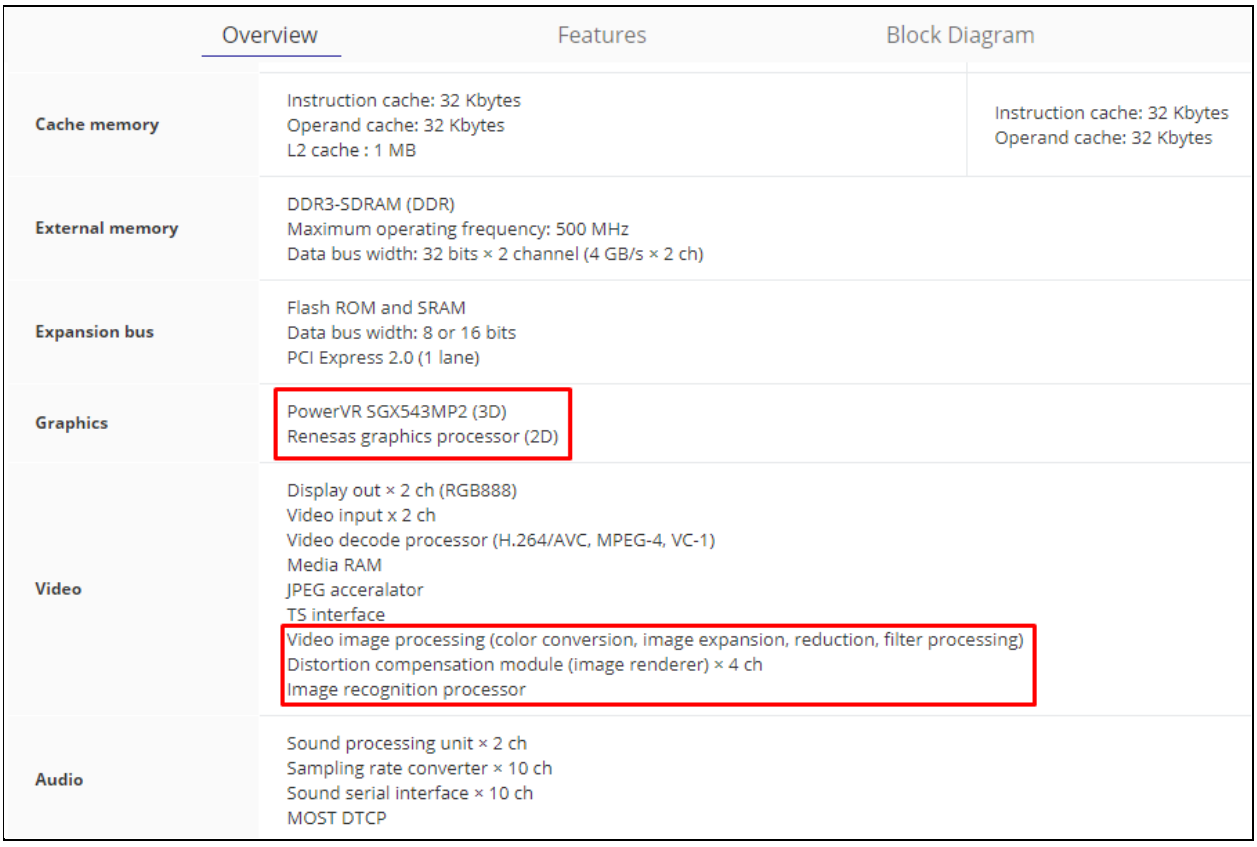


Specification

Item	R-Car H1 Specifications	
Product No.	R-Car H1 (R8A77790)	
Power supply voltage	3.3 V (IO), 1.5 V (DDR3), 1.2 V (Core), 2.5 V (PCIe, MLB), 1.8 V (SDIF UHS-I)	
CPU core	Arm® Cortex®-A9 Quad (with NEON™)	SH-4A core
Maximum operating frequency	1000 MHz	800 MHz
Processing performance	10000 DMIPS	1760DMIPS(Effective), 5600MFLOP
Cache memory	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes L2 cache : 1 MB	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes

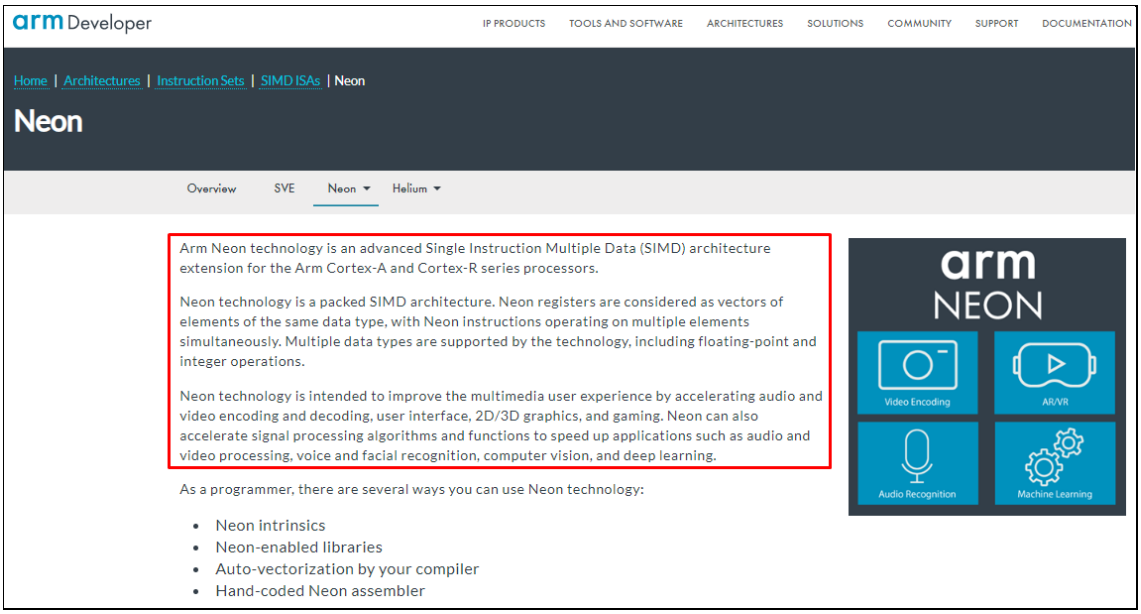
Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as visited on June 29, 2020.



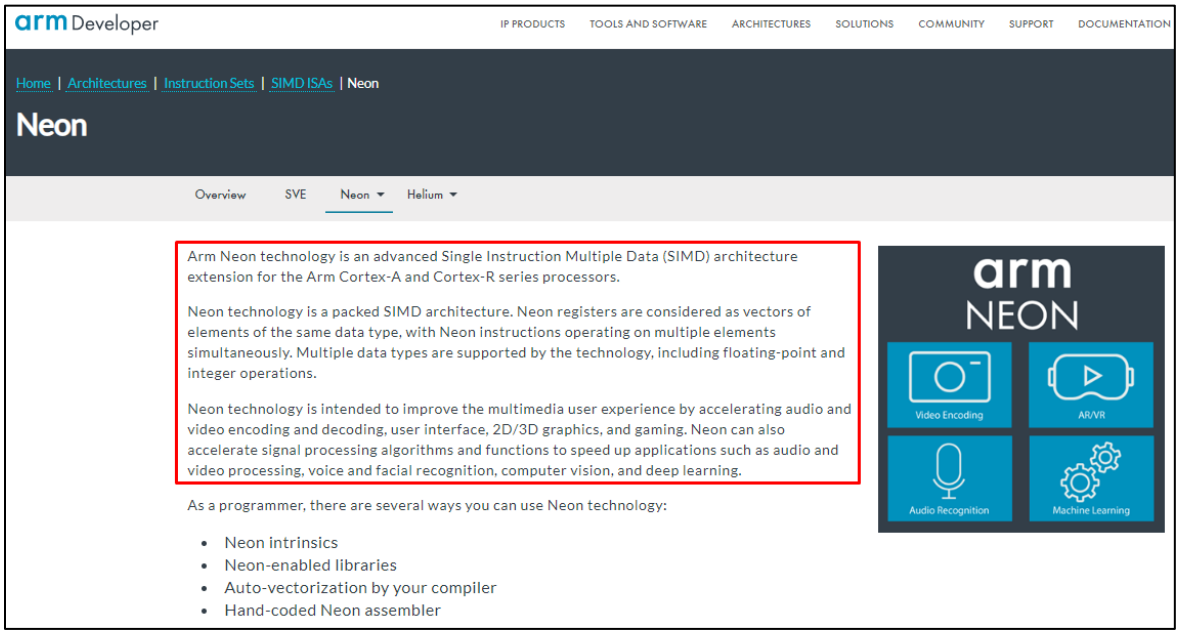
Overview Features Block Diagram

Cache memory	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes L2 cache : 1 MB	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes
External memory	DDR3-SDRAM (DDR) Maximum operating frequency: 500 MHz Data bus width: 32 bits × 2 channel (4 GB/s × 2 ch)	
Expansion bus	Flash ROM and SRAM Data bus width: 8 or 16 bits PCI Express 2.0 (1 lane)	
Graphics	PowerVR SGX543MP2 (3D) Renesas graphics processor (2D)	
Video	Display out × 2 ch (RGB888) Video input x 2 ch Video decode processor (H.264/AVC, MPEG-4, VC-1) Media RAM JPEG acceralator TS interface Video image processing (color conversion, image expansion, reduction, filter processing) Distortion compensation module (image renderer) × 4 ch Image recognition processor	
Audio	Sound processing unit × 2 ch Sampling rate converter × 10 ch Sound serial interface × 10 ch MOST DTCP	

Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as visited on June 29, 2020.



Source: https://developer.arm.com/architectures/instruction-sets/simd-isas/neon, as visited on June 29, 2020.



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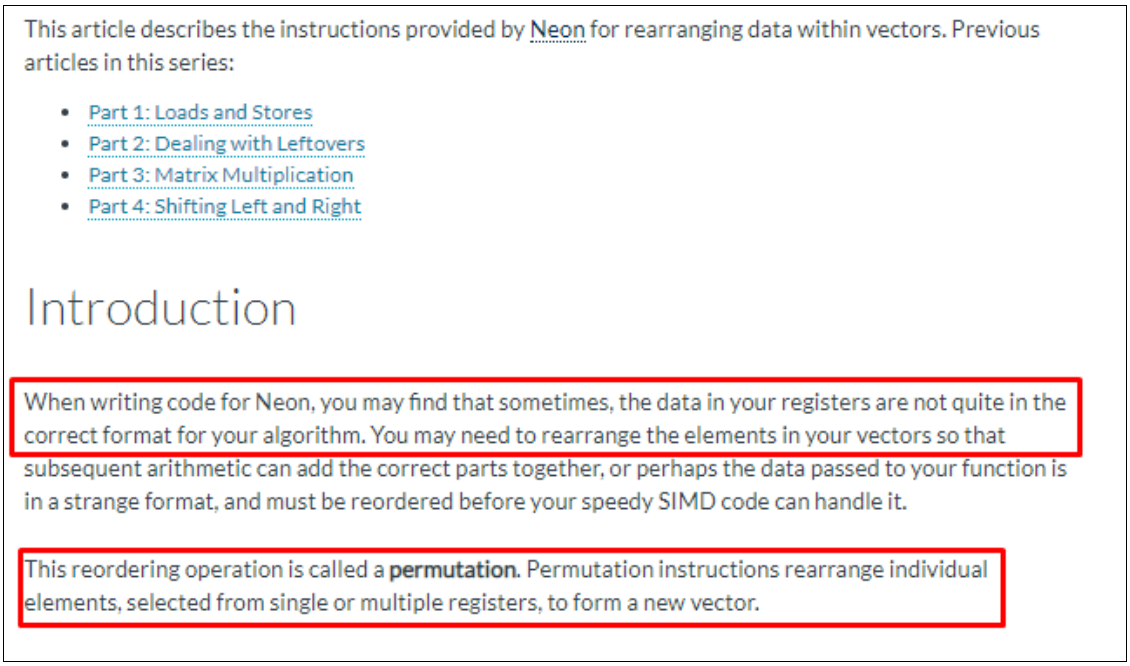


This article describes the instructions provided by Neon for rearranging data within vectors. Previous articles in this series:

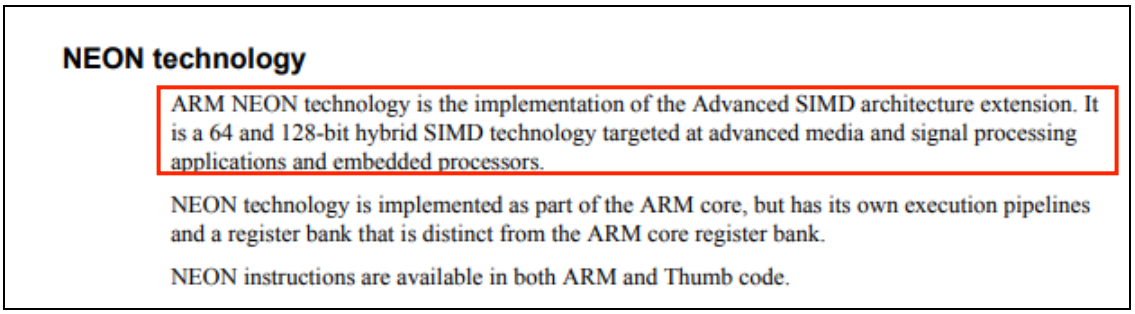
- Part 1: Loads and Stores
- Part 2: Dealing with Leftovers
- Part 3: Matrix Multiplication
- Part 4: Shifting Left and Right

Introduction

When writing code for Neon, you may find that sometimes, the data in your registers are not quite in the correct format for your algorithm. You may need to rearrange the elements in your vectors so that subsequent arithmetic can add the correct parts together, or perhaps the data passed to your function is in a strange format, and must be reordered before your speedy SIMD code can handle it.

This reordering operation is called a **permutation**. Permutation instructions rearrange individual elements, selected from single or multiple registers, to form a new vector.

Source: https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/coding-for-neon---part-5-rearranging-vectors, as visited on June 29, 2020.



NEON technology

ARM NEON technology is the implementation of the Advanced SIMD architecture extension. It is a 64 and 128-bit hybrid SIMD technology targeted at advanced media and signal processing applications and embedded processors.

NEON technology is implemented as part of the ARM core, but has its own execution pipelines and a register bank that is distinct from the ARM core register bank.

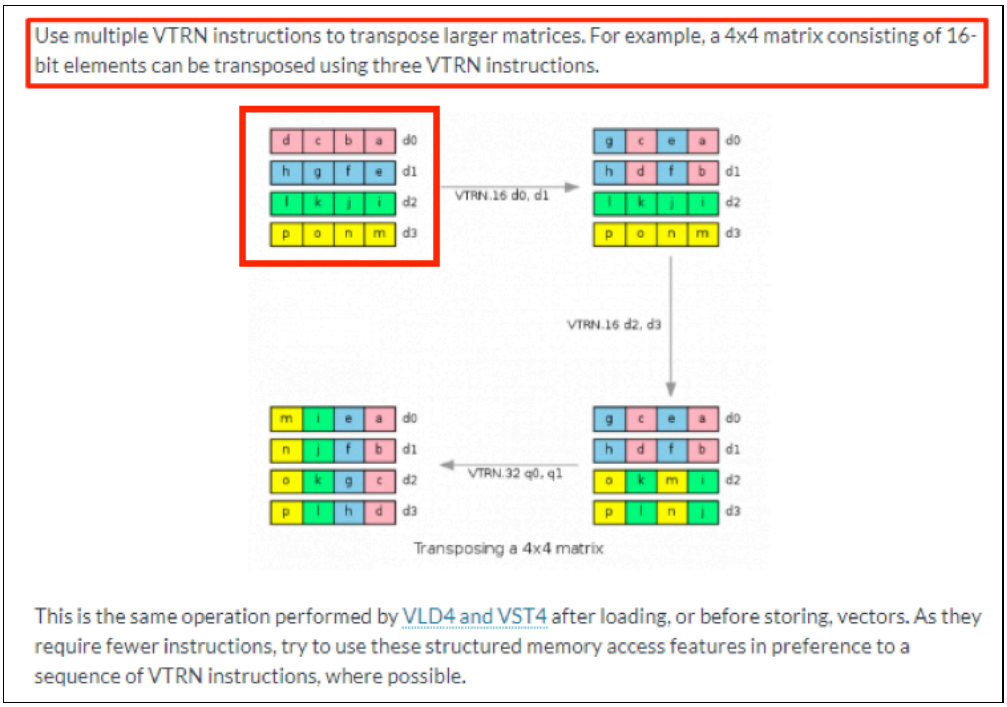
NEON instructions are available in both ARM and Thumb code.

Source: http://infocenter.arm.com/help/topic/com.arm.doc.dui0473j/DUI0473J_armasm_user_guide.pdf, page 40, as visited on June 29, 2020.

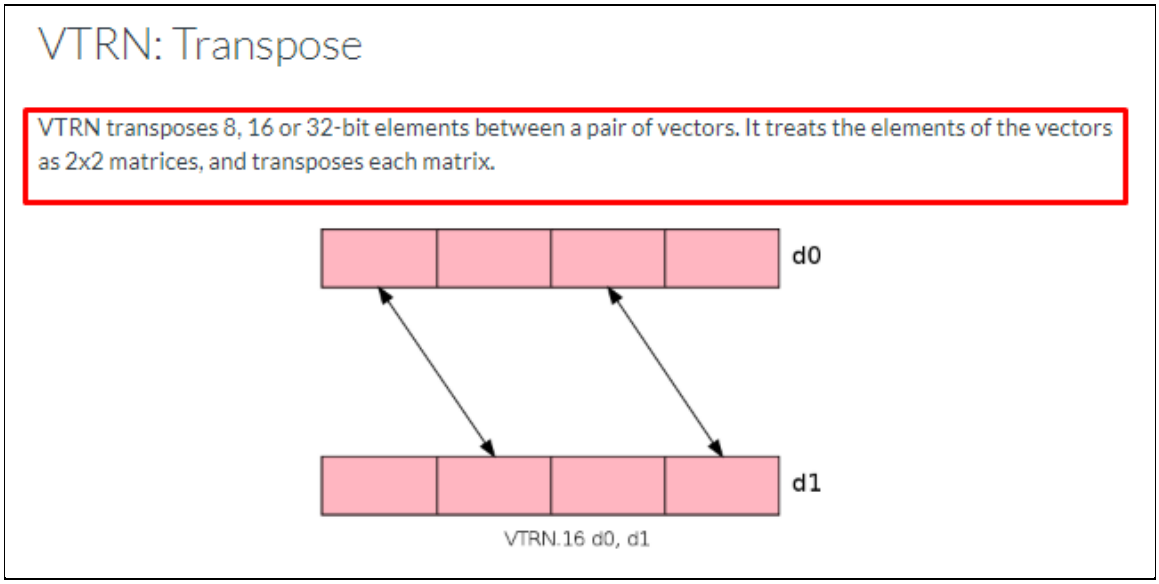
32. Further, Defendants perform and induce others to perform the step of decomposing said two-dimensional data into at least one atomic element said two dimensional data being located in at least one source register said at least one atomic element of said two dimensional data is a 2×2 matrix and said two dimensional data is decomposed into data elements in said matrix.

33. For example, the R-Car H1 SoC uses a permutation instruction (such as a VTRN instruction) and decomposes two-dimensional data (in the form of 4x4 matrix) into a 2x2 matrix.

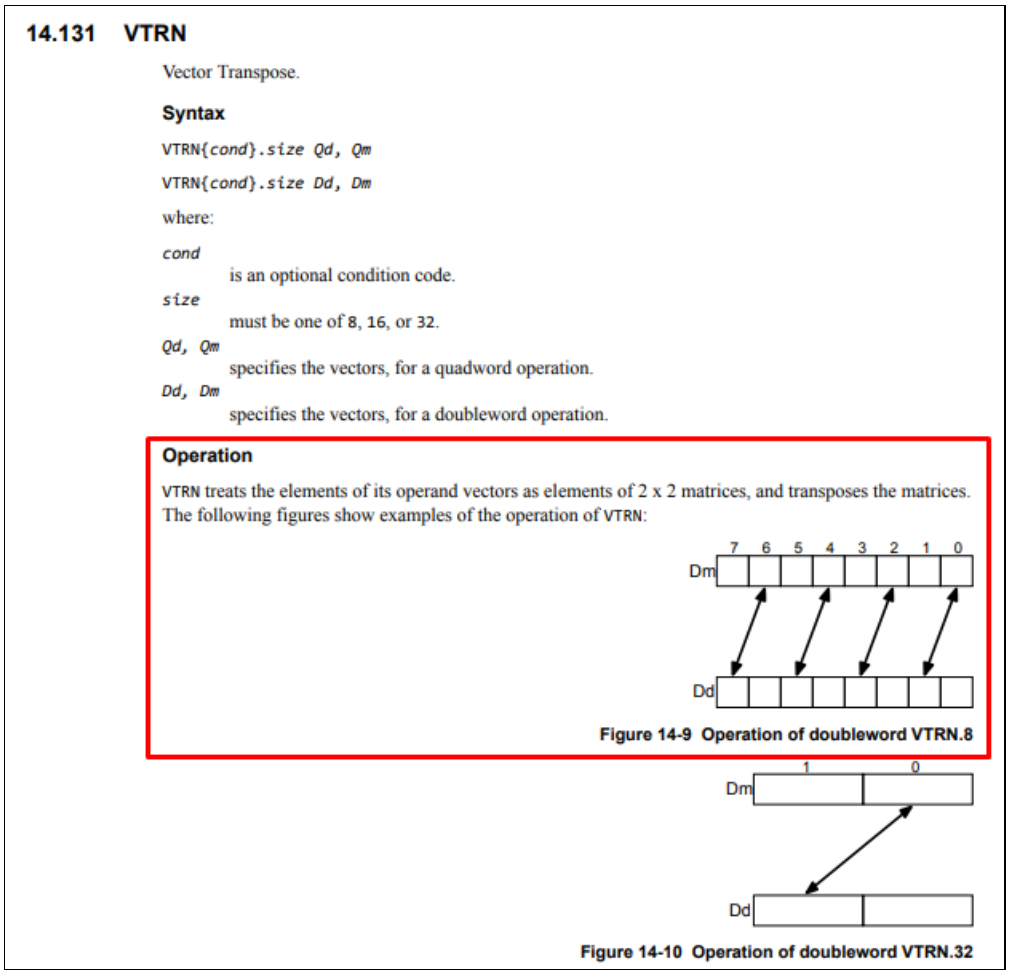
The 4x4 matrix consists of 16-bit elements ("atomic element"). The permutation instruction transposes 8, 16 or 32-bit elements between a pair of vectors. The permutation instruction is applied on the elements of the vectors by dividing it into 2x2 matrices. The two dimensional data is stored in at least one of the d0 and d1 vectors ("source registers").



Source: https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/coding-for-neon---part-5-rearranging-vectors, as visited on June 29, 2020.



Source: https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/coding-for-neon---part-5-rearranging-vectors, as visited on June 29, 2020.



14.131 VTRN

Vector Transpose.

Syntax

`VTRN{cond}.size Qd, Qm`

`VTRN{cond}.size Dd, Dm`

where:

cond
is an optional condition code.

size
must be one of 8, 16, or 32.

Qd, Qm
specifies the vectors, for a quadword operation.

Dd, Dm
specifies the vectors, for a doubleword operation.

Operation

VTRN treats the elements of its operand vectors as elements of 2 x 2 matrices, and transposes the matrices. The following figures show examples of the operation of VTRN:

Figure 14-9 Operation of doubleword VTRN.8

Figure 14-10 Operation of doubleword VTRN.32

Source: http://infocenter.arm.com/help/topic/com.arm.doc.dui0473j/DUI0473J_armasm_user_guide.pdf, page 734, as visited on June 29, 2020.

34. Further, Defendants perform and induce others to perform the step of determining at least one permutation instruction for rearrangement of said data in said atomic element.

35. For example, the R-Car H1 SoC uses a permutation instruction (such as a VTRN instruction) and decomposes two-dimensional data (in the form of 4x4 matrix) into a 2x2 matrix. The permutation instruction transposes ("rearrangement") 8, 16 or 32-bit elements between a

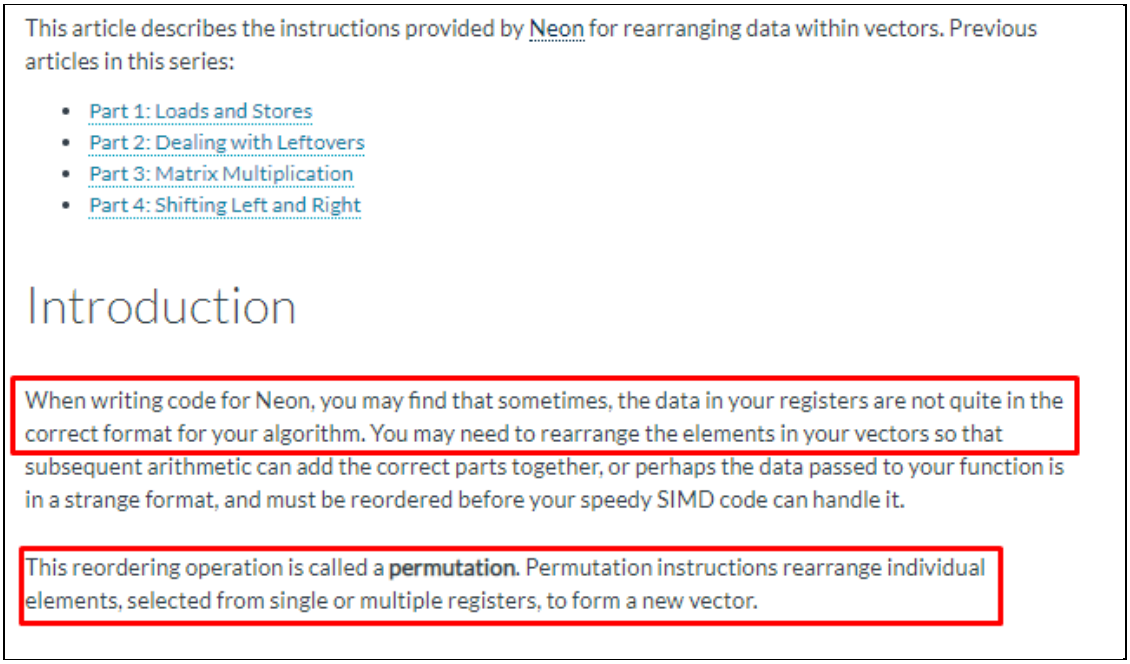
pair of vectors. The permutation instruction is applied on the elements of the vectors by dividing it into 2x2 matrices.

36. Further, Defendants perform and induce others to perform the step of said data elements being rearranged by said at least one permutation instruction, each of said data elements representing a subword having one or more bits.

37. For example, the R-Car H1 SoC uses a permutation instruction (such as a VTRN instruction) and transposes ("rearrange") 8, 16 or 32- bit elements ("subwords") of the 2x2 matrix. The permutation instruction performs subword permutation on each element.

38. Further, Defendants perform and induces others to perform the step of applying said permutation instructions to said subwords and placing said permutated subwords into a destination register.

39. For example, the R-Car H1 SoC uses a permutation instruction (such as a VTRN instruction) and transposes 2x2 matrix elements to form a new vector ("placing said permutated subword into a destination register").



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This reordering operation is called a **permutation**. Permutation instructions rearrange individual elements, selected from single or multiple registers, to form a new vector.

Source: https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/coding-for-neon---part-5-rearranging-vectors, as visited on June 29, 2020.

40. Teleputers has been damaged by Defendants' infringement of the '526 Patent.

COUNT II
(Infringement of U.S. Patent No. 6,952,478B2)

41. Teleputers incorporates the above paragraphs by reference.

42. Defendants have been on notice of the '478 Patent at least as early as the date it received service of this Original Complaint.

43. On information and belief, Defendants have infringed and continue to infringe the '478 Patent by making, using, importing, selling, and/or, offering for sale the Accused Instrumentalities in the United States.

44. On information and belief, Defendants, with knowledge of the '478 Patent, indirectly infringe the '478 Patent by inducing others to infringe the '478 Patent. In particular, Defendants intend to induce customers to infringe the '478 Patent by encouraging customers to use the Accused Instrumentalities in a manner that results in infringement.

45. On information and belief, Defendants also induce others, including customers, to infringe the '478 Patent by providing technical support for the use of the Accused Instrumentalities.

46. On information and belief, at all times Defendants own and control the operation of the Accused Instrumentalities in accordance with an end user license agreement.

47. On information and belief, the Accused Instrumentalities necessarily infringe one or more claims of the '478 Patent when used as intended.

48. On information and belief, the Accused Instrumentalities infringe and induce others to infringe the '478 Patent by providing a method for performing an arbitrary permutation of a

source sequence of bits by defining an intermediate sequence of bits. For example, Defendants infringe at least Claim 1 of the '478 Patent using a permutation instruction, the source sequence of bits are transformed into intermediate sequence of bits. This is repeated using the intermediate sequence of bits as source sequence of bits until a desired sequence of bits is obtained and the permutation instructions form a sequence of instructions. For example, Defendants provide system-on-chip (including but not limited to 88PA6270 SoC, 88PA6220 SoC, PXA1088 SoC, ARMADA 38x, ARMADA 375, ARMADA LP and/or ThunderX3) solutions for parallel data processing.

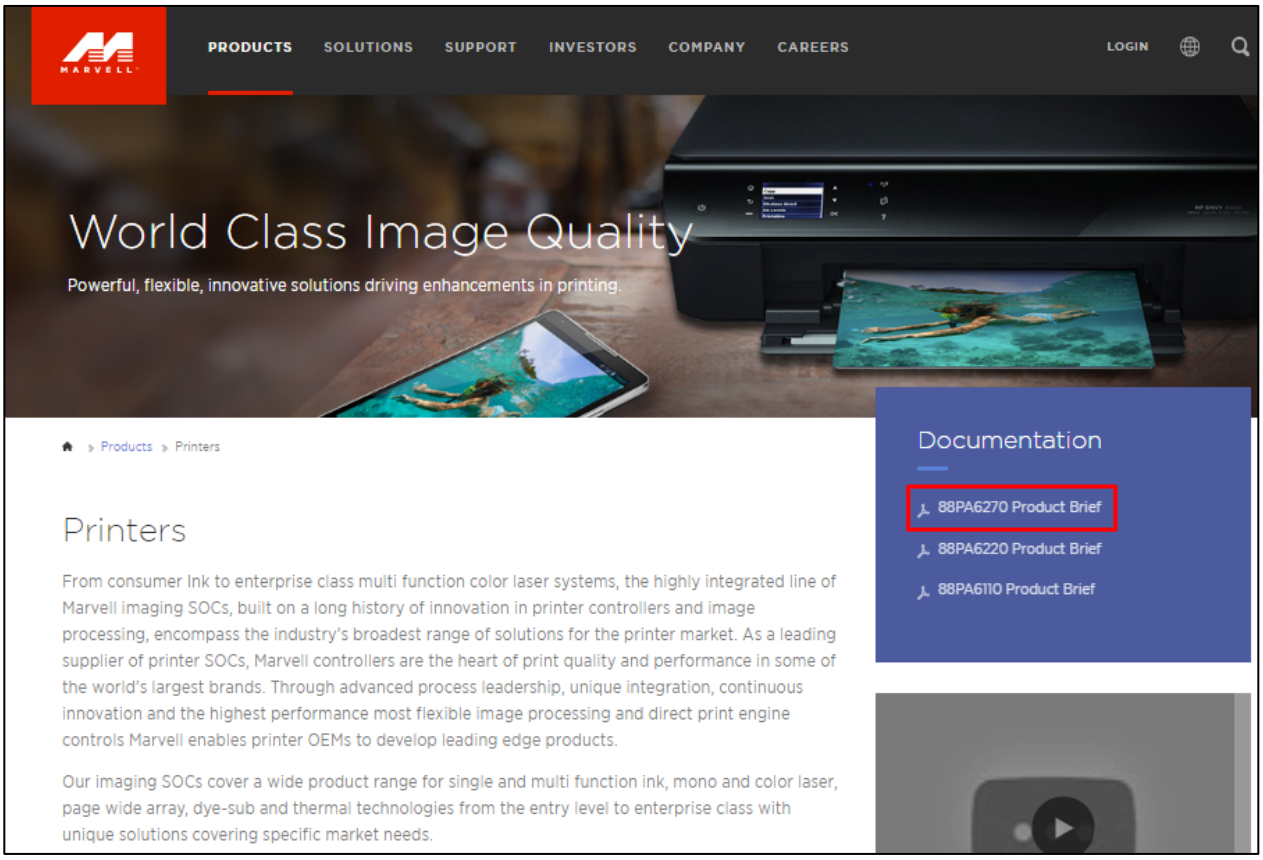
49. For example, Defendants' 88PA6270 SoC (used herein as an exemplary product) is used for class color and monochrome single or multi-function printers. The 88PA6270 SoC includes a quad core 1.2 GHz ARM A53 processor to handle all the application processing and Page Description Language (PDL) rendering requirements.

50. Further, the 88PA6270 SoC ("programmable processor") utilizes ARM Neon technology (a Single Instruction Multiple Data (SIMD) architecture) for improving video encoding and decoding, 2D/3D graphics ("two dimensional (2-D) data"), and/or gaming experience. ARM Neon SIMD architecture provides permutation instructions to rearrange individual elements present in 2D/3D graphics.

51. Further, Defendants directly infringe the claim at least when it tests its SoCs. During such tests, Defendants utilize the SoCs to perform permutation on the input data using permutation instructions available in ARM Neon SIMD ISA (Instruction Set Architecture).

52. Further, Defendants indirectly infringe the claim at least when Defendants' customers (such as device manufacturers which use Defendants' SoCs in their products) perform the method while testing their devices and when the devices are operated by end-users.

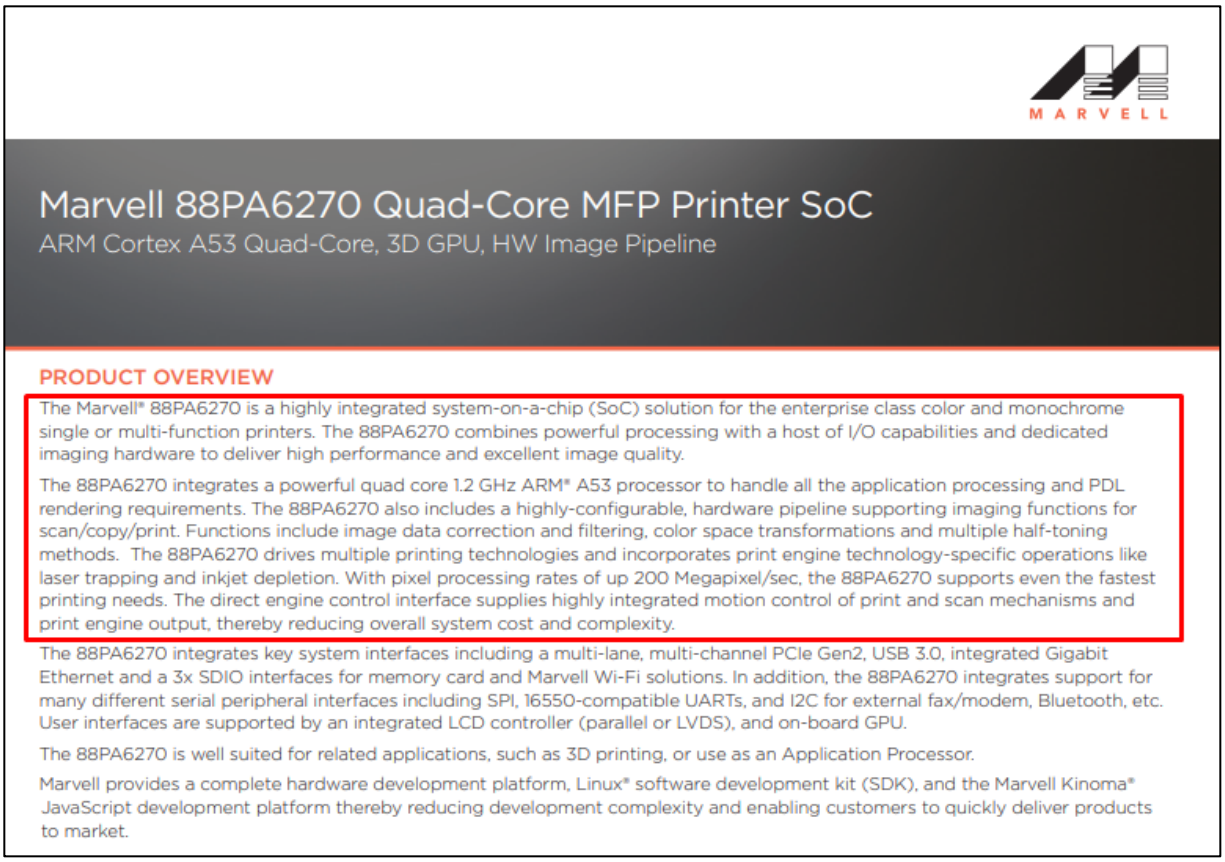
53. Teleputers has been damaged by Defendants' infringement of the '478 Patent.



Source: https://www.marvell.com/products/printers.html, as visited on June 29, 2020.

- **The 88PA6220** powers some of the industry's fastest and highest quality mainstream multi-function printers (MFPs) and copiers supporting a variety of printing technologies, including ink, laser, and LED. This 28nm SoC delivers breakthrough performance at a low system cost by integrating a dual-core ARM® Cortex A53 (64-bit) processor running at 1.0GHz, dual-channel configurable scan and print pipelines, a high-performance 2D/3D GPU, integrated Gigabit Ethernet MAC and PHY, and integrated USB3.0 MAC and PHY.
- **The 88PA6270** is the industry's fastest and most advanced printer system-on-chip (SoC). This 28nm performance-driven SoC integrates a 1.2GHz quad-core ARM® Cortex A53 processor complex, Marvell's industry-leading 32-bit DDR3/4 Memory controller, dual-channel configurable scan and print pipelines, advanced high-speed expansion options, and a high-performance Vivante® 2D/3D GPU. The 88PA6270 will power some of the industry's fastest and highest quality enterprise-class multi-function printers and copiers and integrates support for Ink, Laser, and LED technologies
- **Industry leading solution support:** All Marvell printer SOCs are supported by a hardware development kit (HDK) and software development kit (SDK) reducing the development effort, enabling customers to shorten the development cycle and quickly bring products to market. The Marvell SDK is designed to support a wide array of print technologies including laser, ink, dye-sub and thermal. Precise real time control is essential to producing high quality prints and scanned images. Our SDK incorporates all the necessary real time control to directly drive print engines using high volume production proven algorithms. Using the sample printing, scanning, copying and fax applications developers can easily add their individual features. Connectivity modules are included for all the I/O on the Marvell SOCs as well as Marvell Wi-Fi and user interfaces including color touch screens. The Marvell SDK is available for Linux as well as ThreadX real time operating system.

Source: https://www.marvell.com/products/printers.html, as visited on June 29, 2020.



MARVELL

Marvell 88PA6270 Quad-Core MFP Printer SoC

ARM Cortex A53 Quad-Core, 3D GPU, HW Image Pipeline

PRODUCT OVERVIEW

The Marvell® 88PA6270 is a highly integrated system-on-a-chip (SoC) solution for the enterprise class color and monochrome single or multi-function printers. The 88PA6270 combines powerful processing with a host of I/O capabilities and dedicated imaging hardware to deliver high performance and excellent image quality.

The 88PA6270 integrates a powerful quad core 1.2 GHz ARM® A53 processor to handle all the application processing and PDL rendering requirements. The 88PA6270 also includes a highly-configurable, hardware pipeline supporting imaging functions for scan/copy/print. Functions include image data correction and filtering, color space transformations and multiple half-toning methods. The 88PA6270 drives multiple printing technologies and incorporates print engine technology-specific operations like laser trapping and inkjet depletion. With pixel processing rates of up 200 Megapixel/sec, the 88PA6270 supports even the fastest printing needs. The direct engine control interface supplies highly integrated motion control of print and scan mechanisms and print engine output, thereby reducing overall system cost and complexity.

The 88PA6270 integrates key system interfaces including a multi-lane, multi-channel PCIe Gen2, USB 3.0, integrated Gigabit Ethernet and a 3x SDIO interfaces for memory card and Marvell Wi-Fi solutions. In addition, the 88PA6270 integrates support for many different serial peripheral interfaces including SPI, 16550-compatible UARTs, and I2C for external fax/modem, Bluetooth, etc. User interfaces are supported by an integrated LCD controller (parallel or LVDS), and on-board GPU.

The 88PA6270 is well suited for related applications, such as 3D printing, or use as an Application Processor.

Marvell provides a complete hardware development platform, Linux® software development kit (SDK), and the Marvell Kinoma® JavaScript development platform thereby reducing development complexity and enabling customers to quickly deliver products to market.

Source: https://www.marvell.com/content/dam/marvell/en/public-collateral/printing-solutions/marvell-printers-88pa6270-product-brief-2015-08.pdf, page 1, as visited on June 29, 2020.

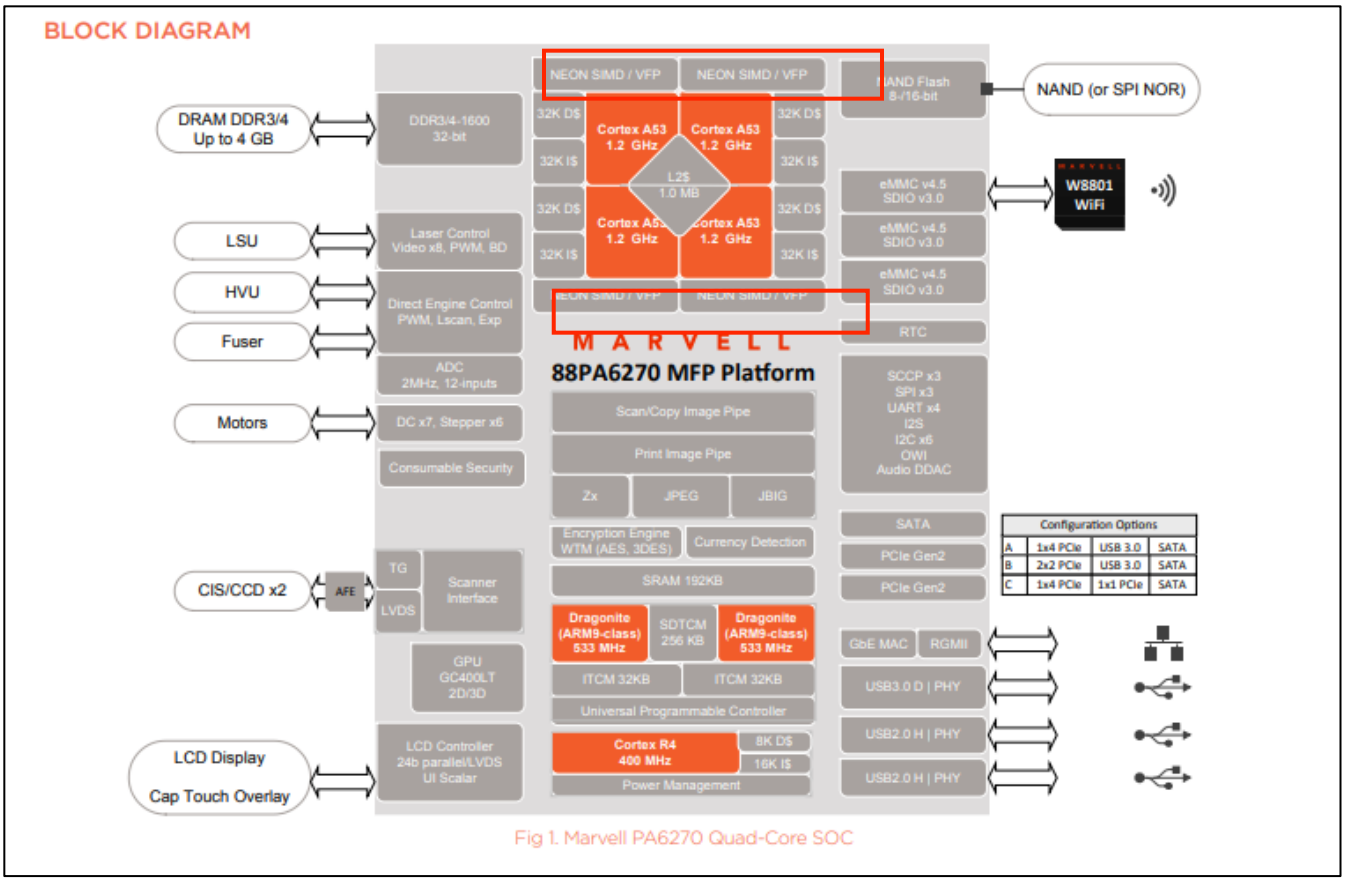


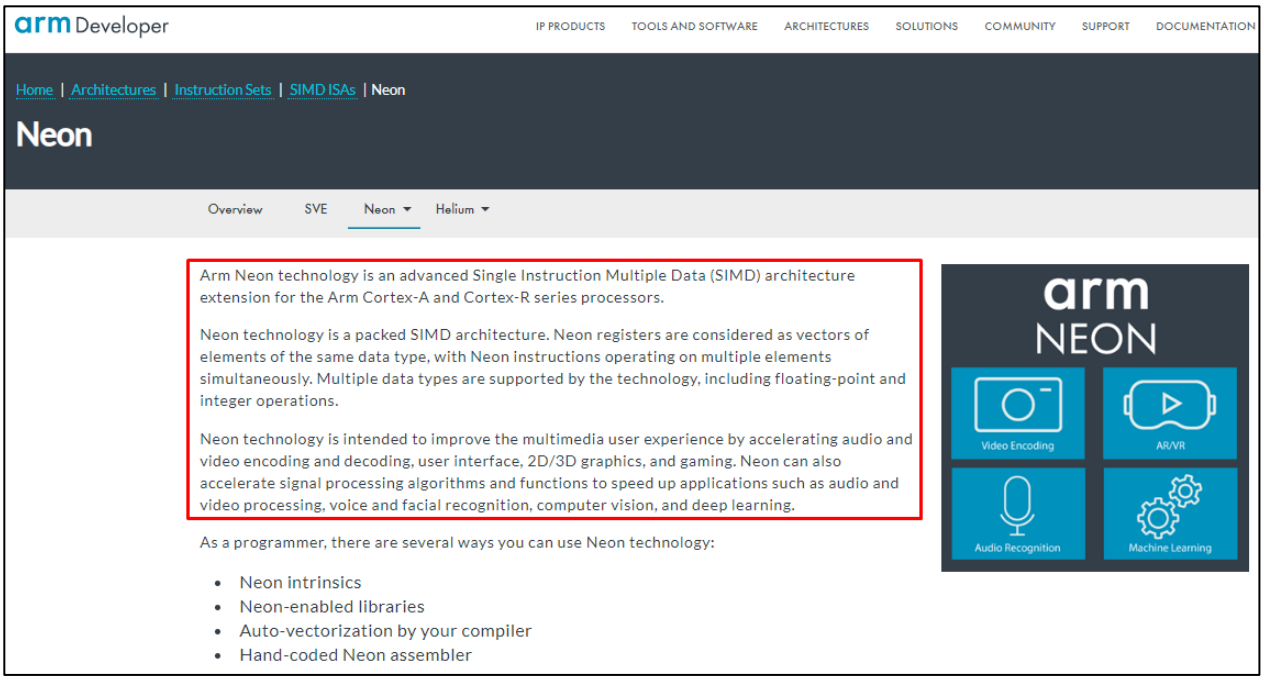
Fig 1. Marvell PA6270 Quad-Core SOC

Source: https://www.marvell.com/content/dam/marvell/en/public-collateral/printing-solutions/marvell-printers-88pa6270-product-brief-2015-08.pdf, page 1, as visited on June 29, 2020.

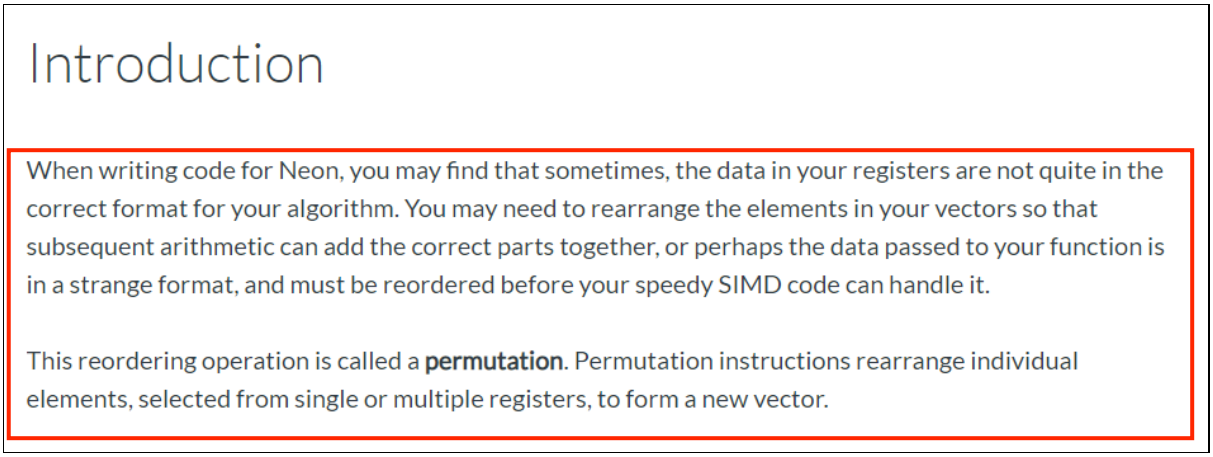
FEATURES AND BENEFITS

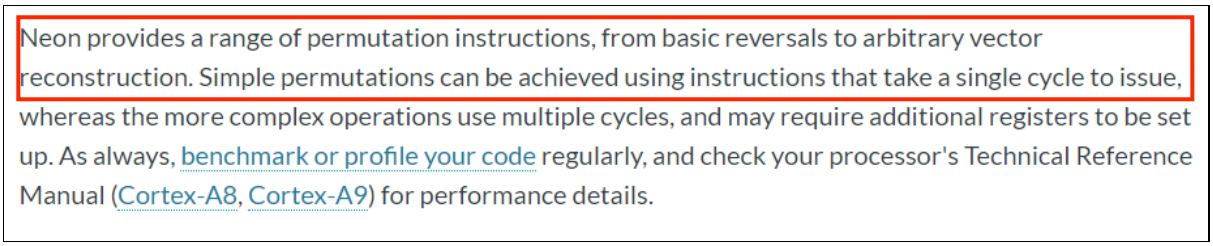
SPECIAL FEATURES	BENEFITS
• CPU	• Leading edge performance with ARM Cortex Quad-Core CPU at 1.2 GHz • NEON™ engine for broad support of media codecs • ARM Cortex R4 for power management, or other tasks while SoC is active • Universal Programmable Controller with 2x ARM9-class processors for dedicated real time control • Secure boot from NAND and eMMC
• Memory	• Advanced 5-port DDR controller with Reordering Buffer (ROB) and pseudo zero-latency write buffer to optimize performance • Up to 4GB DDR3L, DDR4 32-bit provides 1600 MT/s per pin
• GPU	• Vivante GC400LT for smooth 3D and 2D video and graphics • Peak Rate rendering at 30 Mtriangles/s , 0.15 Gpixels/s, and 75 M Vert/sec • Support for industry standard APIs, including OpenGL ES 2.0/1.1, OpenVG 1.1, DirectFB, BLTsville, 2D GAL

Source: https://jp.marvell.com/content/dam/marvell/en/public-collateral/printing-solutions/marvell-printers-88pa6270-product-brief-2015-08.pdf, page 2, as visited on June 29, 2020.

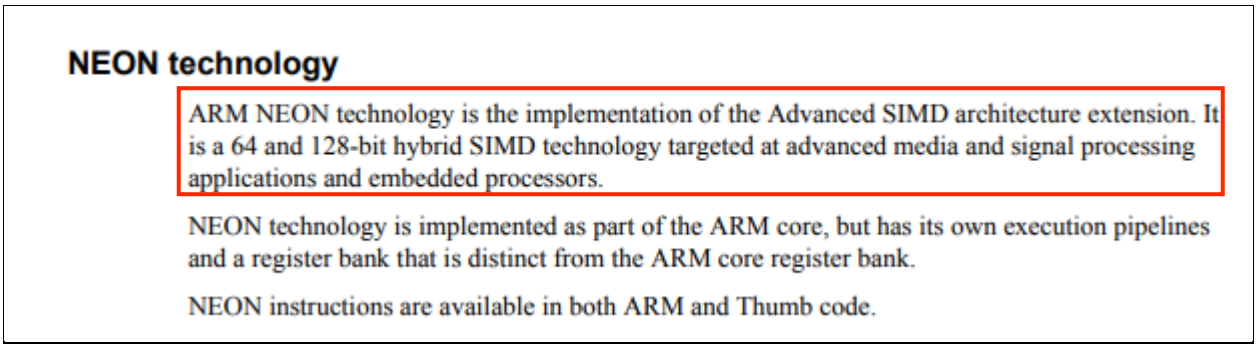


Source: https://developer.arm.com/architectures/instruction-sets/simd-isas/neon, as visited on June 29, 2020.





Source: https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/coding-for-neon---part-5-rearranging-vectors, as visited on June 29, 2020.



NEON technology

ARM NEON technology is the implementation of the Advanced SIMD architecture extension. It is a 64 and 128-bit hybrid SIMD technology targeted at advanced media and signal processing applications and embedded processors.

NEON technology is implemented as part of the ARM core, but has its own execution pipelines and a register bank that is distinct from the ARM core register bank.

NEON instructions are available in both ARM and Thumb code.

Source:
http://infocenter.arm.com/help/topic/com.arm.doc.dui0473j/DUI0473J_armasm_user_guide.pdf, page 2-40, as visited on June 29, 2020.

PRAYER FOR RELIEF

WHEREFORE, Teleputers respectfully requests the Court enter judgment against Defendants:

1. declaring that the Defendants have infringed each of the Patents-in-Suit;

2. awarding Teleputers its damages suffered as a result of Defendants' infringement of the Patents-in-Suit;

3. awarding Teleputers its costs, attorneys' fees, expenses, and interest;

4. awarding Teleputers ongoing post-trial royalties; and

5. granting Teleputers such further relief as the Court finds appropriate.

JURY DEMAND

Teleputers demands trial by jury, under Fed. R. Civ. P. 38.

Dated: June 29, 2020

Respectfully Submitted

/s/ M. Scott Fuller

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